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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1-20 remain.

Claims 1-8, 9-16, and 20 are being amended.

WHAT IS CLAIMED IS:

1. (Currently Amended) A clock signal generator comprising:

input circuitry for receiving an input signal and a clock signal and generating a memory address therefrom;

a memory for storing digital data indexed by said memory address and representing at least a portion of a substantially sinusoidal analog clock signal;

a digital to analog converter for converting data retrieved from said memory to generate said analog clock signal;

a filter for filtering the substantially sinusoidal analog clock to reduce jitter in a binary clock signal derived therefrom; and

circuitry for converting the substantially sinusoidal analog clock signal to the [[a digital output]] binary clock signal such that the binary clock signal has a rate near an integer multiple of a rate of the analog clock signal.

2. (Currently Amended) The clock signal generator of Claim 1 wherein said filter comprises a bandpass filter.

3. (Currently Amended) The clock signal generator of Claim 1 [[2]] wherein said filter comprises a low pass filter.

4. (Currently Amended) The clock signal generator of Claim 1 wherein said memory stores digital data representing real and imaginary parts of a complex waveform.

5. (Currently Amended) The clock signal generator of Claim 4 wherein said filter comprises a bandpass filter.

6. (Currently Amended) The clock signal generator of Claim 1 wherein said circuitry for converting comprises a comparator.

7. (Currently Amended) The clock signal generator of Claim 1 wherein said circuitry for converting comprises a phase-locked loop.

8. (Currently Amended) The clock signal generator of Claim 1 wherein said input circuitry comprises:

a phase-frequency detector comparing the input signal with a reference; and

a delta – sigma noise shaper for filtering at least a selected number of data bits output from said phase-frequency detector to generate selected bits of said memory address.

9. (Currently Amended) A clock signal generator comprising:

a phase detector for comparing a digital input clock signal with a reference signal to generate a digital phase detection signal;

circuitry for generating a memory index from said digital phase detection signal;

a memory storing digital data representing real and imaginary parts of a digital complex waveform accessible by said memory index;

a digital to analog converter for converting digital data accessed from said memory into an analog complex waveform;

bandpass filters for filtering the analog complex waveform to reduce jitter in a binary clock signal derived therefrom; and

a phase locked loop for generating [[a digital output]] the binary clock signal from said analog complex waveform and a complex reference signal, wherein the binary clock signal has a rate near an integer multiple of a rate of said analog complex waveform.

10. (Currently Amended) The clock signal generator of Claim 9 wherein said digital to analog converter comprises:

low pass filters for filtering said real and imaginary parts of said digital complex waveform;

a rotator for rotating said real and imaginary parts of said digital complex waveform by a selected angle such that a noise shaping function of said digital to analog converter tracks a center frequency of said digital output clock; and

quantizers for generating said real and imaginary parts of said analog complex waveform from rotated real and imaginary parts output from said rotator.

11. (Currently Amended) The clock signal generator of Claim 10 wherein said digital to analog converter further comprises a feedback loop including a second rotator for feeding back a rotated output of said quantizer to inputs of said low pass filters.

12. (Currently Amended) The clock signal generator of Claim 10 wherein said bandpass filters each comprise at least one continuous time filter stage.

13. (Currently Amended) The clock signal generator of Claim 12 wherein said continuous time filter stages comprises at least one resonator including at least one variable transconductance.

14. (Currently Amended) The clock signal generator of Claim 9 wherein said digital to analog converter comprises a delta sigma converter.

15. (Currently Amended) The clock signal generator of Claim 9 wherein said circuitry for generating a memory index comprises a noise shaper for shaping noise output from said phase detector to reduce a size of said memory.

16. (Currently Amended) A method of generating a binary [digital] clock signal of a selected frequency comprising the steps of:

storing digital data representing at least a portion of a selected waveform;

selectively retrieving the digital data in response to an input signal;

generating an analog waveform of the selected frequency from the retrieved digital data;

filtering the analog waveform to remove noise and reduce jitter on the binary clock signal; and

converting the analog waveform into the binary [[digital]] clock signal of near an integer multiple of the selected frequency.

17. (Original) The method of generating of Claim 16 wherein the analog waveform comprises a sinewave form and said step of filtering comprises the step of low pass filtering.

18. (Original) The method of generating of Claim 16 wherein said step of storing comprises the step of storing digital data representing at least a portion of a complex waveform and said step of generating comprises the step of generating a complex analog waveform.

19. (Original) The method of generating of Claim 18 wherein said step of filtering comprises the step of bandpass filtering.